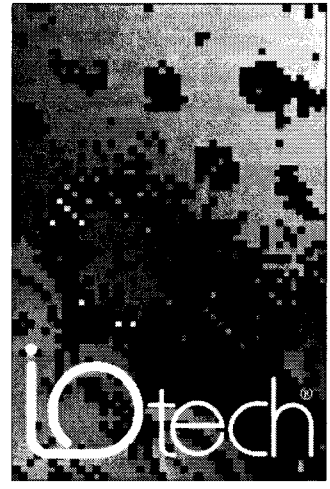
COM232/2AT

RS-232 Communications Adapter



IOtech, Inc.
25971 Cannon Road
Cleveland, OH 44146
Phone: (440) 439-4091
Fax: (440) 439-4093
E-mail: sales@iotech.com
Internet: http://www.iotech.com

COM232/2AT
User's Manual

p/n **256-0921** Rev. **1.0**

Warranty

Your IOtech warranty is as stated on the *product warranty card*. You may contact IOtech by phone, fax machine, or e-mail in regard to warranty-related issues.

Phone: (440) 439-4091, fax: (440) 439-4093, e-mail: sales@iotech.com

Limitation of Liability

IOtech, Inc. cannot be held liable for any damages resulting from the use or misuse of this product.

Copyright, Trademark, and Licensing Notice

FCC Statement

IOtech devices emit radio frequency energy in levels compliant with Federal Communications Commission rules (Part 15) for Class A devices. If necessary, refer to the FCC booklet *How To Identify and Resolve Radio-TV Interference Problems* (stock # 004-000-00345-4) which is available from the U.S. Government Printing Office, Washington, D.C. 20402.

CE Notice

Many IOtech products carry the CE marker indicating they comply with the safety and emissions standards of the European Community. As applicable, we ship these products with a Declaration of Conformity stating which specifications and operating conditions apply.

Warnings and Cautions

Refer all service to qualified personnel. This caution symbol warns of possible personal injury or equipment damage under noted conditions. Follow all safety standards of professional practice and the recommendations in this manual. Using this equipment in ways other than described in this manual can present serious safety hazards or cause equipment damage.

This warning symbol is used in this manual or on the equipment to warn of possible injury or death from electrical shock under noted conditions.

This ESD caution symbol urges proper handling of equipment or components sensitive to damage from electrostatic discharge. Proper handling guidelines include the use of grounded anti-static mats and wrist straps, ESD-protective bags and cartons, and related procedures.

Specifications and Calibration

Specifications are subject to change without notice. Significant changes will be addressed in an addendum or revision to the manual. As applicable, IOtech calibrates its hardware products to published specifications. Periodic hardware calibration is not covered under the warranty and must be performed by qualified personnel as specified in this manual. Improper calibration procedures may void the warranty.

Quality Notice

IOtech has maintained ISO 9001 certification since 1996. Prior to shipment, we thoroughly test our products and review our documentation to assure the highest quality in all aspects. In a spirit of continuous improvement, IOtech welcomes your suggestions.

Table of Contents

COM232/2AT User's Manual

1.1 Introduction

The COM232/2AT is a dual channel RS-232 asynchronous serial communications adapter for systems implementing a 16-bit ISA compatible I/O bus. Data is communicated through two shielded D-9 connectors which provide greater shielding from environmental noise.

The serial interface is implemented with a pair of 16450 Asynchronous Communication Elements (ACEs). The 16450 is compatible with the 8250 ACE found in the original IBM PC/XT models. The optional 16550 ACE provides an additional FIFO mode of operation which reduces CPU overhead at higher data rates.

The COM232/2AT allows independent addressing of each channel through a set of address decode switches (SW1 through SW4). These switches allow each channel to be addressed anywhere in the available I/O address space of the system (0000H through FFFFH). Each channel is also capable of selecting and/or sharing one of eleven possible interrupt request (IRQ) lines (IRQ 2-7, 10-12, 14-15).

NOTE

The optional 16550 ACE has been installed within your IOtech COM232/2AT board.

1.2 Board Description

The first communication channel of the COM232/2AT is controlled by the 16450 labeled U10, switches SW1 and SW2 for addressing, jumper 3 for interrupt request selection, jumper J5 for output signal assignement, and is output through the connector labeled CN1. The second channel is controlled by the 16450 labeled U11, switches SW3 and SW4 for addressing, jumper J4 for interrupt request selection, jumper J6 for output channel assignement, and is output through the connector labeled CN2.

1.3 Specifications

Bus interface: IBM 16-bit bus (AT)

Dimensions: 8.3" x 3.9"

Controllers: 2 - 16450 Asynchronous Communication Elements (ACEs)

(Optional 16550 ACEs)

RS-232 Interface: 2 - D-9 connectors (mal)

Optional: 2 - D-25 connectors (male) using adapter cable provided

Transmit drivers: MC1488 or compatible
High Level Output Voltage: +9V (min), +10.5V (max)
Low Level Output Voltage: -9V (min), -10.5V (max)
Current Limited Output: +/-10mA(typ)
Switching Speed: 55nS(typ), 100nS(max)

Receive Buffers: MC1489 or compatible
High Level Intput Voltage Range: +3 to +13 volts
Low Level Intput Voltage Range: -3 to -13 volts
Switching Speed: 120nS(typ), 175nS(max)
Switching Speed: 55nS(typ), 100nS(max)

I/O Address range: See Figure 16
Interrupt levels: IRQ 2(9), 3-7, 10-12, 14-15
Power requirements:

IT	IMS	Supply
390mA	443mA	+5 Volts
38mA	46mA	+12 Volts
36mA	43mA	-12 Volts

I_T - Typical adapter current

I_{MS} - Maximum statistical adapter current

1.4 16450/16550 Functional Description

The 16450 is an improved specification version of the 8250 Asynchronous Communications Element (ACE) found in the original IBM PC and PC/XT systems and is functionally equivalent to the 8250. This ACE performs serial-to-parallel conversion on data charaters received from an external device and parrallel-to-serial conversion on data characters received from the PC's CPU.

The functional programming is done by the system software via a 3-state 8-bit bi-directional data bus; this inlcudes the on-board baud rate generator. A description of the control registers will be given throughout this manual.

Other features of the 16450/16550 include:

- Programmable baud rate, character length, parity, and number of stop bits.
- Automatic addition and removal of start, stop, and parity bits.
- Independent and prioritized transmit, receive and status interrupts.
- Transmitter clock output to drive receiver logic
- External receiver clock input.

The following pages provide a brief summary of the internal registers available within the 16450 and 16550 ACEs. The registers are addressed as shown in the table below. Registers specific to the 16550 will be marked with an asterisk(*).

DLAB	A2	A1	A0	Register Description
0	0	0	0	Receive buffer (read only) Transmitter holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only) FIFO control* (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (LSB)
1	0	0	1	Divisor latch (MSB)

NOTE: DLAB is accessed through the Line Control Register.

Figure 1: Internal Register Map for 16450 & 16550 ACEs

1.4.1 Interrupt Enable Register

The bit definitions for this register are as follows:

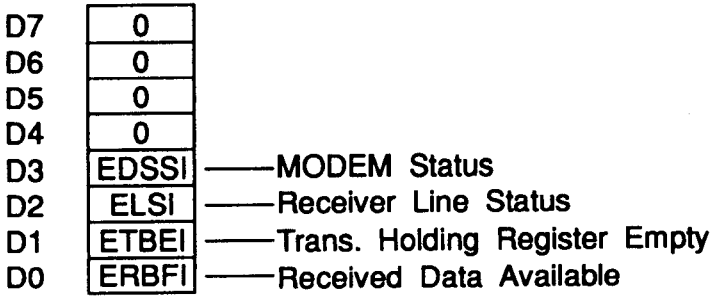


Figure 2: Interrupt Enable Register Definitions

EDSSI MODEM Status Interrupt:	When set (logic 1), enables interrupt on clear to send, data set ready, ring indicator, and data carrier detect.
ELSI Receiver Line Status Interrupt:	When set (logic 1), enables interrupt on overrun, parity, framing errors, and break indication.
ETBEI Transmitter Holding Register Empty Interrupt:	When set (logic 1), enables interrupt on transmitter register empty.
ERBFI Received Data Available Interrupt:	When set (logic 1), enables interrupt on received data available or FIFO trigger level.

* For Optional 16550 only.

1.4.2 Interrupt Identification Register

The bit definitions for this register as as follows:

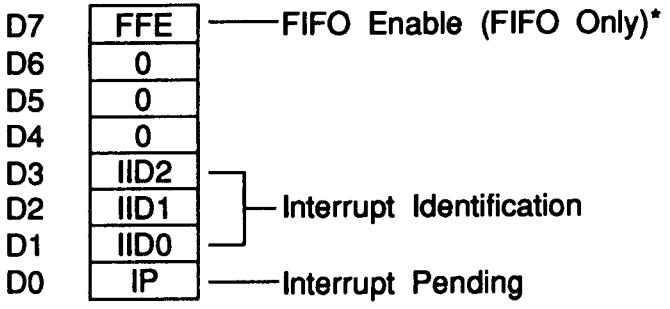


Figure 3: Interrupt Identification Register Definitions

FFE FIFO Enable:*	When logic 1, indicates FIFO mode enabled.
IIDx Interrupt Identification:	Indicates highest priority interrupt pending if any. See IP and figure 5. NOTE: IID2 is always a logic 0 in the 16450 and in the 16550 character mode.
IP Interrupt Pending:	When logic 0, indicates that an interrupt is pending and the contents of the interrupt identification register may be used to determine the interrupt source. See IIDx and figure 4.

* For Optional 16550 only.

IID2	IID1	IID0	IP	Priority	Interrupt Type
x	x	x	1	N/A	None
0	1	1	0	Highest	Receiver Line Status
0	1	0	0	Second	Received Data Ready
1	1	0	0	Second	Character Timeout* (FIFO only)
0	0	1	0	Third	Transmitter Holding Register Empty
0	0	0	0	Fourth	MODEM Status

Figure 4: Interrupt Identification Bit Definitions

Receiver Line Status:	Indicates overrun, parity, framing errors or break interrupts. The interrupt is cleared by reading the line status register.
Received Data Ready:	Indicates receiver data available. The interrupt is cleared by reading the receiver buffer register.
FIFO mode:*	Indicates the receiver FIFO trigger level has been reached. The interrupt is reset when the FIFO drops below the trigger level.
Character Timeout:* (FIFO mode only)	Indicates no characters have been removed from or input to the receiver FIFO for the last four character times and there is at least one character in the FIFO during this time. The interrupt is cleared by reading the receiver FIFO.
Transmitter Holding Register Empty:	Indicates the transmitter holding register is empty. The interrupt is cleared by reading the interrupt identification register or writing to the transmitter holding register.
MODEM Status:	Indicates clear to send, data set ready, ring indicator, or data carrier detect have changed state. The interrupt is cleared by reading the MODEM status register.

* For Optional 16550 only.

1.4.3 FIFO Control Register

For Optional 16550 Only

The bit definitions of this register are as follows:

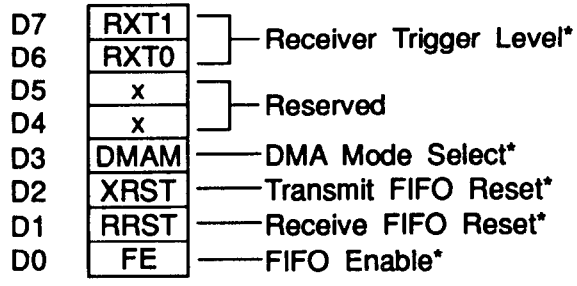


Figure 5: FIFO Control Register

RXTx - Receiver FIFO Trigger Level:*	Determines the trigger level for the FIFO interrupt as given in the table below.

RXT1	RXT0	Trigger Level (bytes)
0	0	1
0	0	4
1	0	8
1	1	14

Figure 6: FIFO Trigger Levels

DMAM DMA Mode Select:*	When set (logic 1), RxRDY and TxRDY change from mode 0 to mode 1. DMA mode is not supported on COM232/2AT.
XRST Transmit FIFO Reset:*	When set (logic 1), all bytes in the transmitter FIFO are cleared and the counter is reset. The shift register is not cleared. XRST is self-clearing.
RRST Receive FIFO Reset:*	When set (logic 1), all bytes in the receiver FIFO are cleared and the counter is reset. The shift register is not cleared. RRST is self-clearing.
FE FIFO Enable:*	When set (logic 1), enables transmitter and receiver FIFOs. When cleared (logic 0), all bytes in both FIFOs are cleared. This bit must be set when other bits in the FIFO control register are written to or the bits will be ignored.

* For Optional 16550 only.

1.4.4 Line Control Register

The bit definitions for this register are as follows:

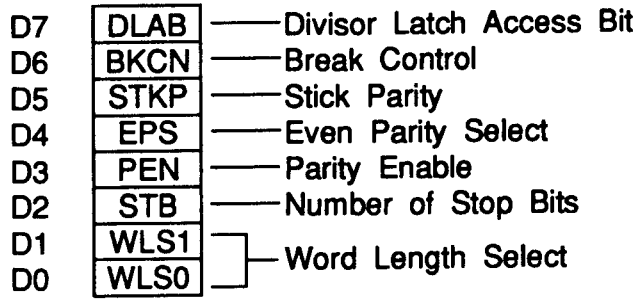


Figure 7: Line Control Register

DLAB Divisor Latch Access Bit:	DLAB must be set to logic 1 to access the baud rate divisor latches. DLAB must be set to logic 0 to access the receiver buffer, transmitting holding register and interrupt enable register.
BKCN Break Control:	When set (logic 1), the serial output (SOUT) is forced to the spacing state (logic 0).
STKP Stick Parity:	Forces parity to logic 1 or logic 0 if parity is enabled. See EPS, PEN, and Figure 8.
EPS Even Parity Select:	Selects even or odd parity if parity is enabled. See STKP, PEN, and Figure 8.
PEN Parity Enable:	Enables parity on transmission and verification on reception. See EPS, STPK, and Figure 8.

STKP	EPS	PEN	Parity
x	x	0	None
0	0	1	Odd
0	1	1	Even
1	0	1	Logic 1
1	1	1	Logic 2

Figure 8: 16450/16550 Parity Selections

STB Number of Stop Bits:	Sets the number of stop bits transmitted. See WLSx and Figure 9.

WLSx Word Length Select:	Determines the number of bits per transmitted word. See STB and Figure 9.

STB	WLS1	WLS0	Word Length	Stop Bits
0	0	0	5 bits	1
0	0	1	6 bits	1
0	1	0	7 bits	1
0	1	1	8 bits	1
1	0	0	5 bits	1 1/2
1	0	1	6 bits	2
1	1	0	7 bits	2
1	1	1	8 bits	2

Figure 9: Word Length and Stop Bit Selections

1.4.5 Modem Control Register

The bit definitions for this register are as follows:

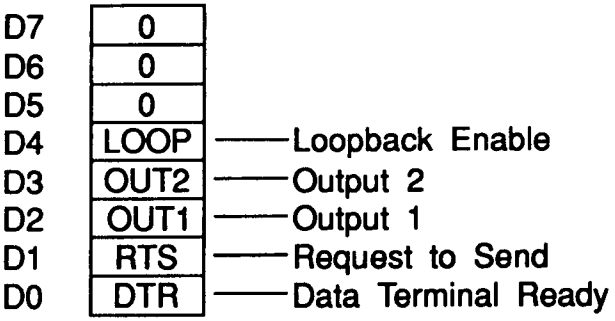


Figure 10: MODEM Control Register Definitions

LOOP Loopback Enable:	When set (logic 1), the transmitter shift register is connected directly to the receiver shift register. The MODEM control inputs are internally connected to the MODEM control outputs and the outputs are forced to the inactive state. Therefore all characters transmitted are immediately received to verify transmit and receive data paths. Transmitter and receiver interrupts still operate normally. MODEM control interrupts are available but are now controlled through the MODEM control register.

Bits OUT2, OUT1, RTS, and DTR perform identical functions on their respective outputs. When these bits are set (logic 1) in the register, the associated output is forced to a logic 0. When cleared (logic 0), the output is forced to a logic 1.

OUT2 Output 2:	Controls the OUT2 output, pin 31, as described above. Used for interrupt enable. See Section 1.8.
OUT1 Output 1:	Controls the OUT1 output, pin 34, as described above.
RTS Request To Send:	Controls the RTS output, pin 32, as described above.
DTR Data Terminal Ready:	Controls the DTR output, pin 33, as described above.

1.4.6 Line Status Register

The bit definitions for this register are as follows:

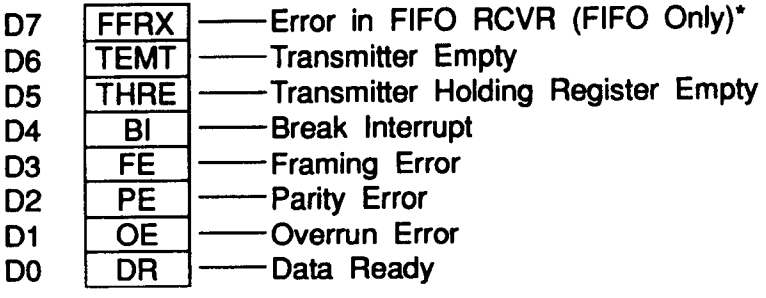


Figure 11: Line Status Register Definitions

FFRX FIFO Receiver Error:*	Always a logic 0 in character mode.
FIFO mode:	Indicates one or more parity errors, framing errors, or break indications in the receiver FIFO. FFRX is reset by reading the line status register.
TEMT Transmitter Empty:	Indicates the transmitter holding register (or FIFO*) and the transmitter shift register are empty and are ready to receive new data. TEMT is reset by writing a character to the transmitter holding register.
THRE Transmitter Holding Register Empty:	Indicates the transmitter holding register (or FIFO*) is empty and it is ready to accept new data. THRE is reset by writing data to the transmitter holding register.

* For Optional 16550 only.

Bits BI, FE, PE, and OE are the sources of receiver line status interrupts. The bits are reset by reading the line status register. In FIFO mode*, these bits are associated with a specific character in the FIFO and the exception is revealed only when that character reaches the top of the FIFO.

BI Break Interrupt:	Indicates the receive data input has been in the spacing state (logic 0) for longer than one full word transmission time.
FIFO mode:*	Only one zero character is loaded into the FIFO and transfers are disabled until SIN goes to the mark state (logic 1) and a valid start bit is received.
FE Framing Error:	Indicates the received character had an invalid stop bit. The stop bit following the last data or parity bit was a 0 bit (spacing level).
PE Parity Error:	Indicates that the received data does not have the correct parity.
OE Overrun Error:	Indicates the receive buffer was not read before the next character was received and the character is destroyed.
* FIFO mode:	Indicates the FIFO is full and another character has been shifted in. The character in the shift register is destroyed but is not transferred to the FIFO.

DR Data ready:	Indicates data is present in the receive buffer (or FIFO*). DR is reset by reading the receive buffer register.

* For Optional 16550 only.

1.4.7 Modem Status Register

The bit definitions for this register are as follows:

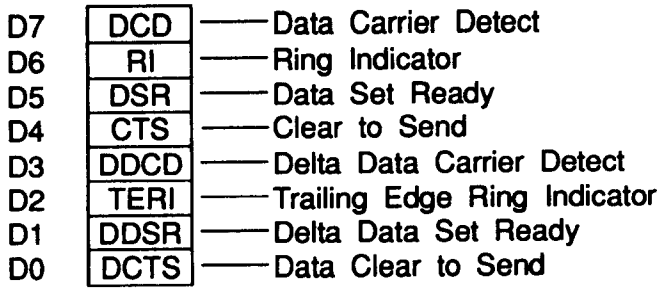


Figure 12: MODEM Status Register Definitions

DCD Data Carrier Detect:	Complement of the DCD input, pin 38.
RI Ring Indicator:	Complement of the RI input, pin 39.
DSR Data Set Ready:	Complement of the DSR input, pin 37.
CTS Clear To Send:	Complement of the CTS input, pin 36.

Bits DDCD, TERI, DDSR, and DCTS are the sources of MODEM status interrupts. These bits are reset when the MODEM status register is read.

DDCD Delta Data Carrier Detect:	Indicates the Data Carrier Detect input, pin 38, has changed state.

TERI Trailing Edge Ring Indicator:	Indicates the Ring Indicator input, pin 39, has changed from a low to a high state.
DDSR Delta Data Set Ready:	Indicates the Data Set Ready input, pin 37, has changed state.
+DCTS Delta Clear To Send:	Indicates the Clear to Send input, pin 36, has changed state.

1.4.8 Scratchpad Register

This register is not used by the 16450 or 16550 ACEs. It may be used by the programmer for data storage.

1.5 FIFO Interrupt Mode Operation

For Optional 16550 Only

1. The receive data interrupt is issued when the FIFO reaches the trigger level. The interrupt is cleared as soon as the FIFO falls below the trigger level.
2. The interrupt identification register's receive data available indicator is set and cleared along with the receive data interrupt above.
3. The data ready indicator is set as soon as a character is transferred into the receiver FIFO and is cleared when the FIFO is empty.

1.6 Baud Rate Selection

The 16450 UART determines the baud rate of the serial output using a combination of the input clock frequency and the values contained in the divisor latches. Standard PC, PC/XT, PC/AT, and PS/2 serial interfaces use an input clock of 1.8432 Mhz. To increase versatility, the COM232/2AT uses an 18.432 Mhz crystal and a frequency divider circuit to produce the standard input clock frequency.

Jumper J1 is used to set the frequency input to the 16450/16550. It may be connected to divide the clock input by 1, 2, 5, or 10. For compatibility, J1 should be configured to divide by 10 as shown in figure 13(d). A table of baud rates available using the 1.8432 Mhz input is given in figure 14.

* For Optional 16550 only.

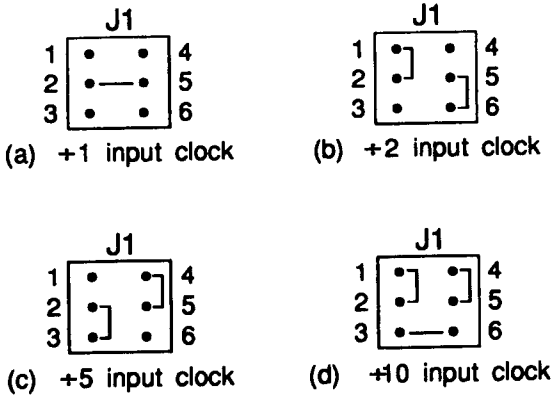


Figure 13: Input Clock Frequency Options

NOTE: For compatibility, the jumper should be set at +10 (18.432 Mhz +10 = 1.8432 Mhz).

The following table lists divisor latch settings for common baud rates using an 1.8432 Mhz input clock. For compatibility, connect jumper in the divide by 10 configuration (figure 13(d)).

Desired Baud Rate	Divisor Latch Value	Error Between Desired and Actual Value (5)
50	2304	—
75	1536	—
110	1047	0.026
150	768	—

300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

Figure 14: Divisor Latch Settings

1.7 Addressing

The COM232/2AT uses 8 consecutive I/O address locations in the range of 0 to FFFF Hex. The card uses 13 address selection switches to determine its base address. The sixth switch of SW2 and SW4 will Enable (ON) or Disable (OFF) that particular channel.

The switch position "ON" corresponds to address bit "0" whereas the switch position "OFF" corresponds to address bit "1". The example illustrating the switch setting for the card is shown in the following figure.

Optional Address	
3F8H	Serial 1
2F8H	Serial 2
3220H	Serial 3
3228H	Serial 4
4220H	Serial 5
4228H	Serial 6
5220H	Serial 7
5228H	Serial 8

The figure below shows an address selection of channel 1. The address is set for 03F8H.

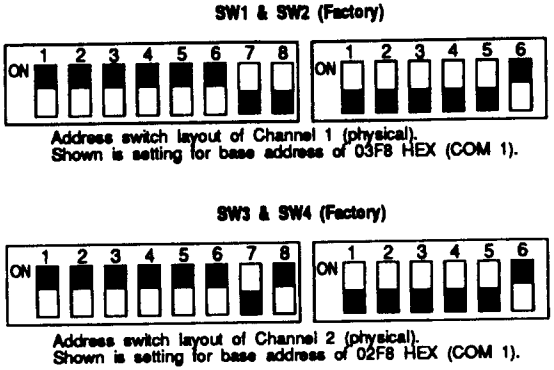


Figure 15: Factory Address Switch Settings

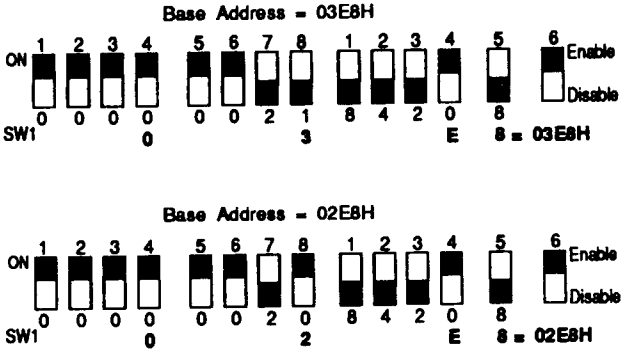


Figure 16: Address Switch Selection Examples

1.8 Interrupts

Each channel of the COM232/2AT may independently select one of eleven possible interrupt request levels (IRQ 2-7, 10-12, 14-15). The interrupt request level is selected using jumper J3 for channel 1 and jumper J4 for channel 2 as shown in the figure below.

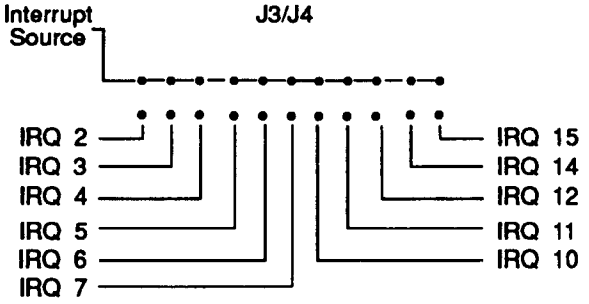
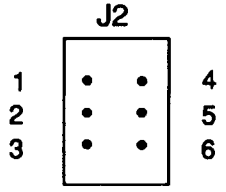


Figure 17: Interrupt Level Selection Jumper

One additional feature of the COM232/2AT is the ability to share one interrupt level between both communication channels, or to share an interrupt level with another IOtech adapter supporting this interrupt sharing feature. Jumper J2 controls the COM232/2AT's interrupt sharing capability.



J2	Interrupt Operation	
Channel 1	1-2 2-3	Dedicated interrupt level Interrupt sharing enabled
Channel 2	4-5 5-6	Dedicated interrupt level Interrupt sharing enabled

NOTE: To be 100% ISA compatible, jumper J2 must be set to the dedicated interrupt level positions.

1.9 Output Configurations

RS-232-C devices are classified by their function as either Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). Generally, data terminal equipment is defined as the communication source while data communication equipment is defined as devices that provide a communication channel between two DTE type devices.

The figure below shows the use of Data Terminal Equipment (DTE) and Data Communication Equipment (DCE) to implement an RS-232-C communication link.

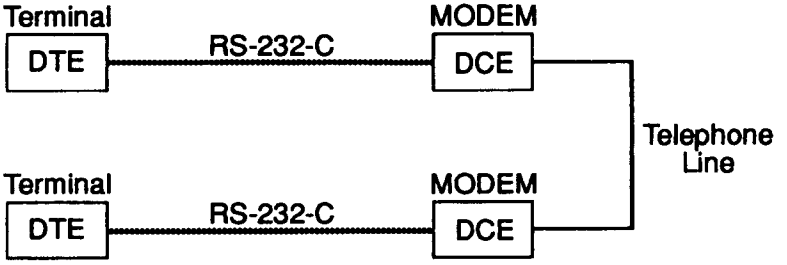
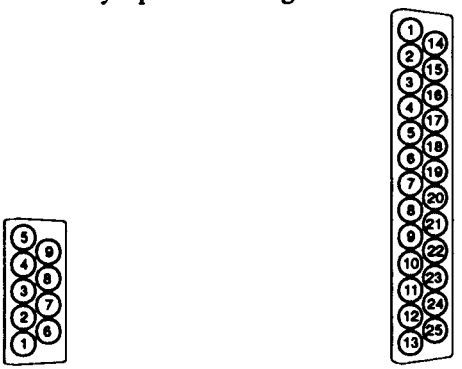


Figure 20: RS-232-C Communication Link

Data terminal equipment and data communication equipment have complementary pinouts to allow terminals and MODEMs to be connected directly using a one-to-one cable as shown in the D-9 connector pinout in the figure below. In many applications, DCEs are unnecessary because of the short distances involved. In these cases, a custom cable called a NULL MODEM or MODEM eliminator is usually required to perform the direct connection of two DTEs. A typical null MODEM cable is shown in the DB-25 connector in figure 21. To further simplify these connections, the COM232/2AT is equipped with a DTE/DCE jumper configuration block for each channel. This allows the COM232/2AT to communicate with DCE or DTE device without any special cabling.



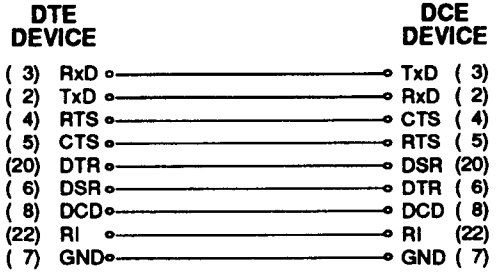
D-9 Connector (CN1 & CN2)

D-25P Connector (Adapter Cable Output)

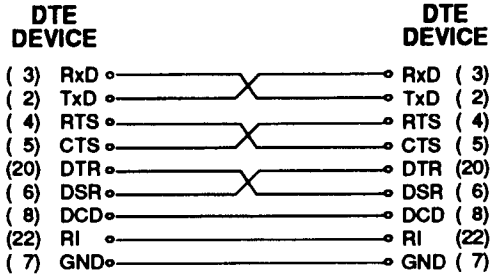
Figure 21: Output Connectors

RS-232-C Description		DTE Connection		DCE Connection	
		D-9	D-25	D-9	D-25
Data Carrier Detect	(DCD)	1	8	1	8
Receiver Data	(RxD)	2	3	3	2
Transmit Data	(TxD)	3	2	2	3
Data Terminal Ready	(DTR)	4	20	6	6
Signal Ground		5	7	5	7
Data Set Ready	(DSR)	6	6	4	20
Request to Send	(RTS)	7	4	8	5
Clear to Send	(CTS)	8	5	7	4
Ring Indicator	(RI)	9	22	9	22

Figure 22: Connector Definitions for RS-232-C



Typical DTE to DCE Cable



Typical DTE to DTE Cable (null MODEM)

Figure 23: Cabling Requirements for RS-232 Devices

Refer to the figure below for the COM232/2AT output configuration jumper for port 1.

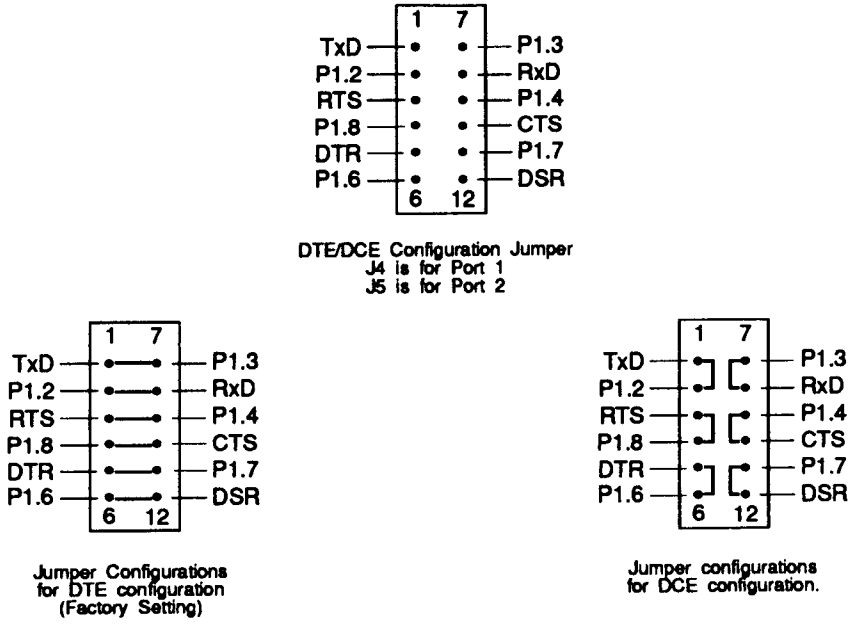


Figure 24: Output Configuration Jumpers

NOTE: Connections are referenced by port and pin number. For example, P1.3 = port 1 pin 3, P1.6 = port 1 pin 6.

1.10 Hardware Installation

1. Set addressing, interrupts and output configuration jumpers on the card.
2. Turn unit off.
3. Remove system cover as instructed in the computer reference guide.
4. Insert card into a vacant slot following the guidelines for installation.
5. Replace system cover.
6. Plug computer into wall outlet.

1.11 Software Installation

1.11.1 DOS Installation

This section briefly describes some of the files contained on the installation disk. Particularly:

- COMDRIVE.SYS
- QMODE.COM
- QCFG.EXE

The files on this disk are intended to be used with IOtech's multi-port ASYNC boards.

COMDRIVE.SYS

This program is installed with CONFIG.SYS and should be located at [C:\COMDRIVE.SYS]. COMDRIVE allows for the use of COM1 through COM34 as DOS devices. This means that 'COPY *.* COM5' (assuming that the board is there and it is configured) would work through DOS. COMDRIVE is written to be used with IOtech's multi-port async boards.

To install COMDRIVE.SYS add the following line to your CONFIG.SYS file:

```
device=C:\COMDRIVE.SYS
```

(or the actual location of the program COMDRIVE.SYS.)

QCFG.EXE

This program is used to maintain the COMDRIVE device driver.

The port addresses of COMDRIVE are configurable and need to be defined before any multi-port board will operate properly with QMODE.COM and DOS. After the multi port board is installed into the PC, COMDRIVE.SYS needs to be configured to recognize it. To do this the base address of the installed multi-port board(s) needs to be known.

Let's assume that the multi-port board has a base address of 300H (default), and let's also assume that it is a COM232/4PC QUAD PORT board. This would put port 1 of the board at a base address of 300H,port 2=308H, port 3=310H, and port 4=318H. Lastly, assume standard COM1 and COM2 boards are already installed in the PC.

To get COM3 up and running enter 'COM3=300' from the command line of QCFG. This will pipe data that goes from DOS COM3 to IOtech's multi-port board port 1. Then, to get COM4 activated, the command 'COM4=308' needs to be issued from QCFG, and so on for all other ports that are available.

QMODE.COM

This utility is used to configure COM1-COM34. It operates like the DOS MODE command. To use QMODE the syntax is:

```
QMODE COMn[:]baud[,[parity][,[length][,[stopbits]
```

where:

n of COMn is 1 - 34 for the proper async logical port

baud: 110,150,300,600,1200,2400,4800,or 9600 (only first 2 characters required, ie. "96")

parity: E(ven) (default), N(one), O(dd)

length: 7 (default), 8

stopbits: 1 (default), 2

Example: QMODE COM18:2400,n,8,1

This command will configure logical COM address 18 to be 2400 baud, no parity, 8 bit, 1 stop bit.

1.11.1.1 Installing the Files

1. Add COMDRIVE to the CONFIG.SYS file
   ```
   DEVICE=COMDRIVE.SYS
   ```
2. Reboot, to recognize COMDRIVE.SYS
3. Run QCFG.EXE configure COMDRIVE.
   ```
   COM3=300
   :
   ```
4. Make sure, while in QCFG.EXE, to SAVE your modified configuration
   ```
   SAVE
   Y (answer yes to both questions)
   Y
   :
   ```
5. Add QMODE commands to your AUTOEXEC.BAT for power-up configuration of the new COM PORTS
   ```
   QMODE  COM3:96,e,7,1
   ```
6. Reboot.
7. Now all defined COM ports should be addressable.
   `'COPY  *.*  COM3'` will work properly

1.11.2 Windows Installation

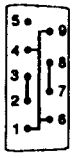
To install the IOtech Windows 3.1 versions of the communications drivers, follow these steps:

1. Select `Run` from either File Manager or Program Manager. This is in the File Menu for either of these.
2. Type `a:\setup`. This works if your source diskette is inserted in drive A. Use the appropriate drive letter of the disk drive for your source diskette.
3. Setup will install the new device drivers and will modify the appropriate Windows system files. There is an additional application, Com Config, which is placed in the IOtech App group file.
4. Run the IOtech Com Config application. This will allow you to configure the device drivers for things such as the I/O address, IRQ, baud rate, handshaking, etc. This application incorporates context sensitive help.

1.12 Troubleshooting

Problem	Possible Solution	
Computer won't boot up?	Check to see if card is plugged in properly.	Remove card and try again. Also try a different slot.
	Check address location.	Check for address conflicts with existing expansion cards. (See Addressing.) Also try to re-work switches.
	Defective Card	Unauthorized repair voids warrent, contact the factory.
Unable to communicate?	Check cable connections.	See section on Output Configurations.
	Check address location.	Check for legal address location (See Addressing). Also try to re-work switches.
	Check all jumper configurations.	Check J2 & J3 for proper interrupt level. Check J4 & J5 for proper configuration.
	Check operation.	Most computers have diagnostics for Com1 and COM2 (factory setting). See figure below for an example of a Loop-Back connector.
		Unauthorized repair voids warrent, contact the factory.

*DB-9 Female Connector is required



Signal Ground		Ring Indicator	
Data Terminal Ready		Clear to Send	
Transmit Data		Request to Send	
Receive Data		Data Set Ready	
Data Carrier Detect			

Connect Pins	
3 & 2	(TxD - RxD)
7 & 8	(RTS - CTS)
1 & 4 & 6 & 9	(DCD - DTR - DSR - RI)

Figure 25: Loop Back Connector